RESEARCH ARTICLE OPEN ACCESS

6T SRAM Cell: Design And Analysis

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ABSTRACT
SRAM has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power, low voltage memory design during recent years due to increase demand for notebooks, laptops, IC memory cards and hand held communication devices. SRAMs are widely used for mobile applications as both on chip and off-chip memories, because of their ease of use and low standby leakage.
The main objective of this paper is evaluating performance in terms of Power consumption, delay and SNM of existing 6T CMOS SRAM cell in 45nm and 180nm technology.
Keywords **–**6T SRAM cell, Power dissipation, Read Delay, SNM, Write Delay.

I. INTRODUCTION

6T static random-access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered.

II. 6T SRAM CELL OPERATION

1. Standby Mode (the circuit is idle)

In standby mode word line is not asserted (word line=0), so pass transistors N3 and N4 which connect 6t cell from bit lines are turned off. It means that cell cannot be accessed. The two cross coupled inverters formed by N1-N2 will continue to feed back each other as long as they are connected to the supply, and data will hold in the latch.

2. Read Mode (the data has been requested)

In read mode word line is asserted (word line=1), Word line enables both the access transistor which will connect cell from the bit lines. Now values stored in nodes (node a and b) are transferred to the bit lines. Assume that 1 is stored at node a so bit line bar will discharge through the driver transistor (N1) and the bit line will be pull up through the Load transistors (P1) toward VDD, a logical 1. Design of SRAM cell requires read stability (do not disturb data when reading).

3. Write Mode (updating the contents)

Assume that the cell is originally storing a 1 and we wish to write a 0. To do this, the bit line is lowered to 0V and bit bar is raised to VDD, and cell is selected by raising the word line to VDD. Typically, each of the inverters is designed so that PMOS and NMOS are matched, thus inverter threshold is kept at VDD/2. If we wish to write 0 at node a, N3 operates in saturation. Initially, its source voltage is 1. Drain terminal of N2 is initially at 1 which is pulled down by N3 because access transistor N3 is stronger than N1. Now N2 turns on and P1 turns off, thus new value has been written which forces bit line lowered to 0V and bit bar to VDD. SRAM to operate in write mode must have write-ability which is minimum bit line voltage required to flip the state of the cell.

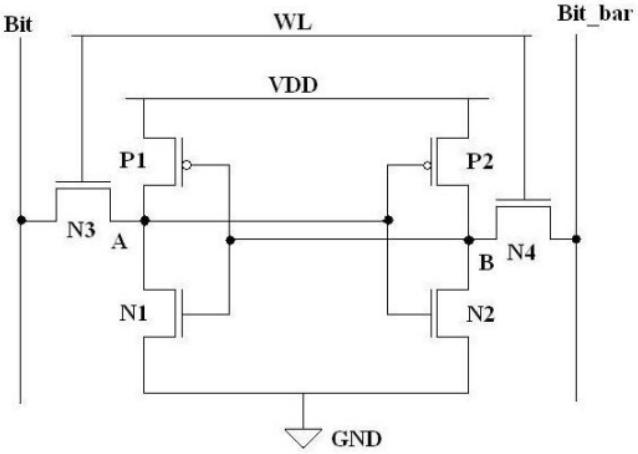

FIGURE 1 Schematic of 6t SRAM cell

III. PERFORMANCE PARAMETERS OF SRAM

SNM**:** maximum dc voltage that the cell tolerates before it changes state in read mode. The size of the maximum square that can be inscribed in butterfly curve gives the SNM of the SRAM cell. Instead of measuring the read stability and write ability separately a method known as N-curve

method by which both parameters can be arrived at simultaneously is used. Hold SNM is the maximum dc noise that the cell tolerates before it changes state in the hold mode.

Write delay**:** It is the delay between the applications of the word line WL signal and the time at which the data is actually written.

Read delay**:** Read delay is the delay involved in allowing the bit lines to discharge by about 10% of the peak value or the delay between the application of the WL signal and the response time of the sense amplifier.

IV. RESULTS AND ANALYSIS

1. 180nm Technology

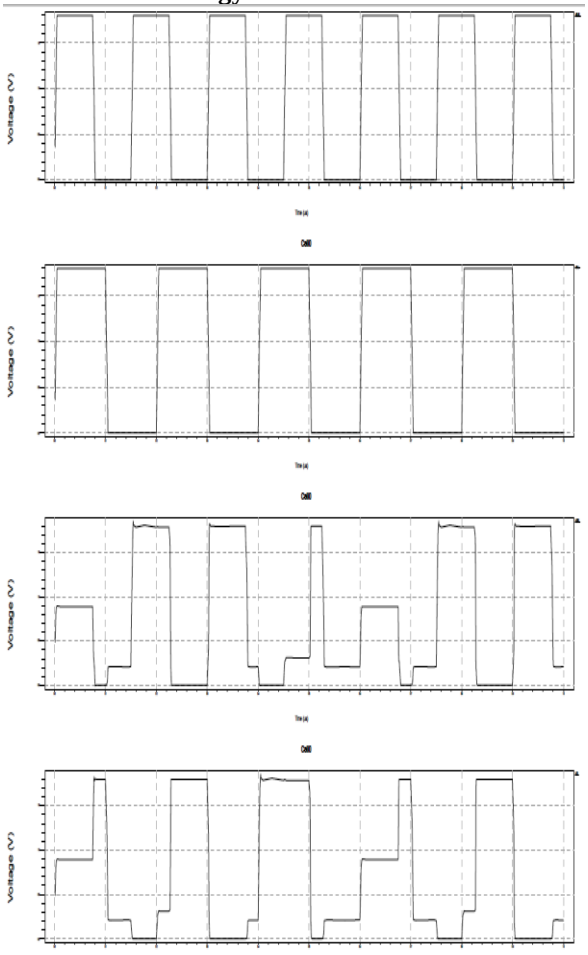

FIGURE 2 Transient analysis at 180nm technology

1. Average power consumed = 1.317488e-004 watts.
2. Read delay = 4.7168e-010 sec.
3. Write delay= 9.6081e-010 sec.
4. Hold SNM=0.5 volt.
5. Read SNM=0.1 volt.
6. Write SNM=0.7 volt.

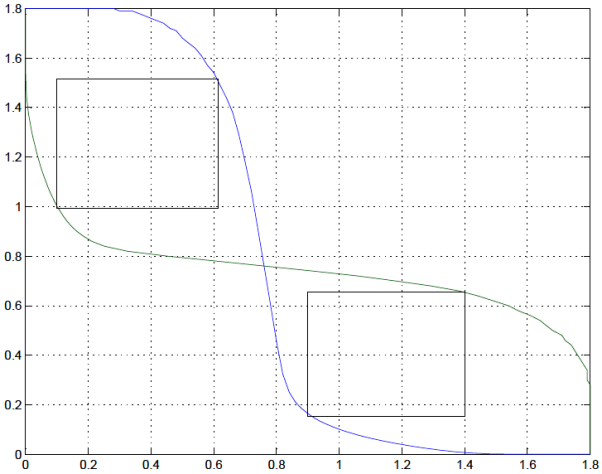

FIGURE 3 Butterfly curve for hold operation at 180nm technology

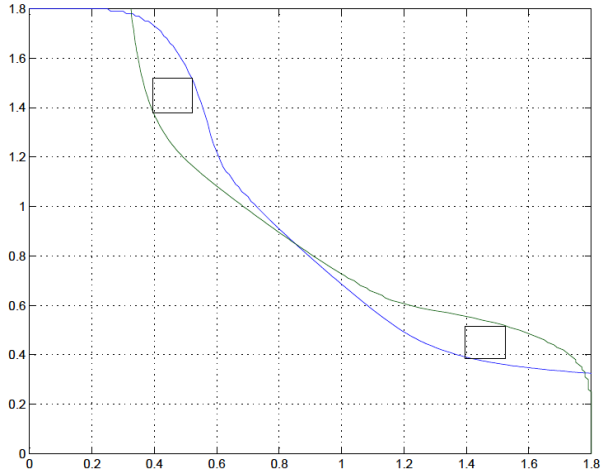

FIGURE 4 Butterfly curve for read operation at 180nm technology

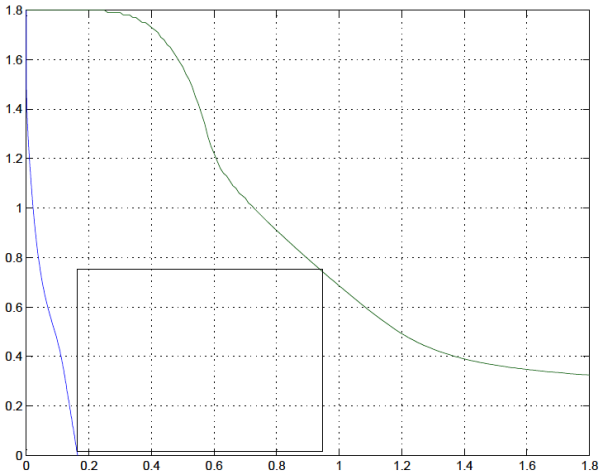

FIGURE 5 Butterfly curve for write operation at 180nm technology

2. 45nmTchnology:

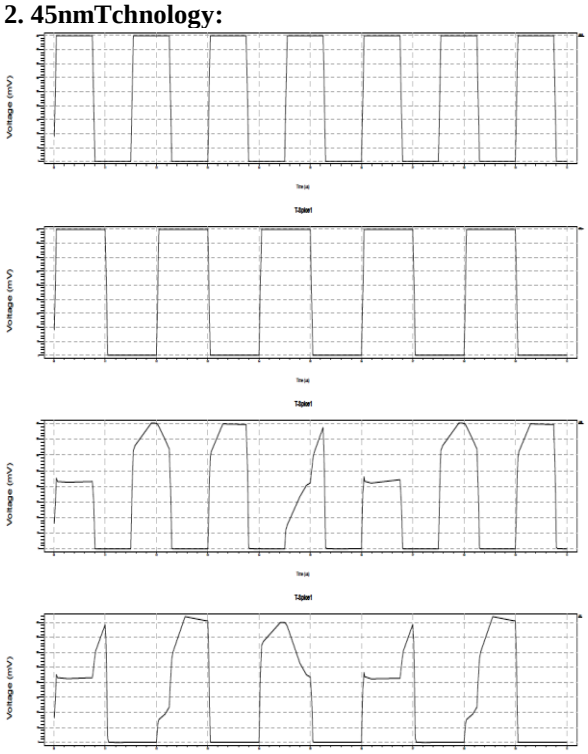

FIGURE 6 Transient analysis at 45nm technology

1. Average power consumed = 8.492199e-010 watts.
2. Read Delay = 4.7222e-010 sec.
3. Write Delay= 2.1395e-009 sec.
4. Hold SNM=0.15 volt.
5. Read SNM=0.05 volt.
6. Write SNM=0.2 volt.

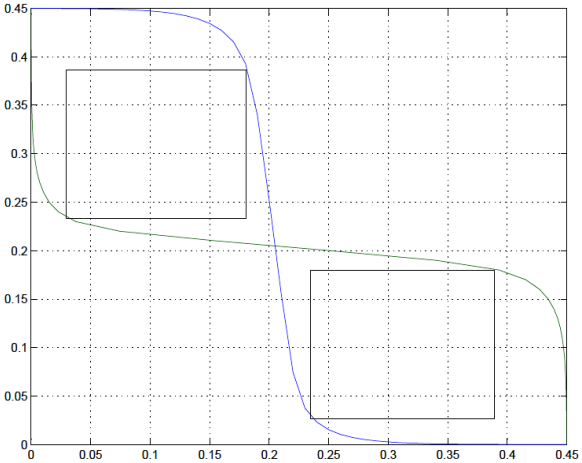

FIGURE 7 Butterfly curve for hold operation at 45nm technology

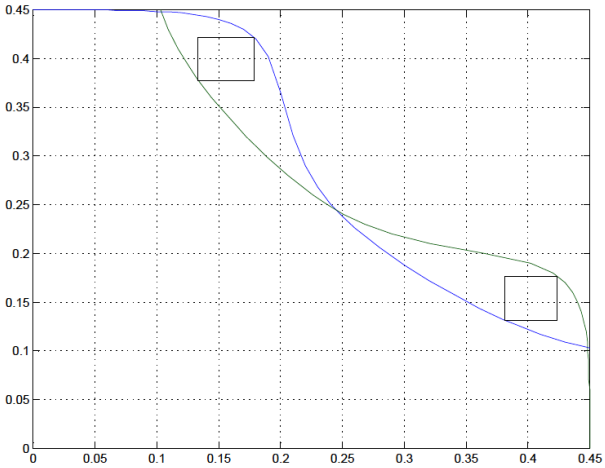

FIGURE 8 Butterfly curve for read operation at 45nm technology

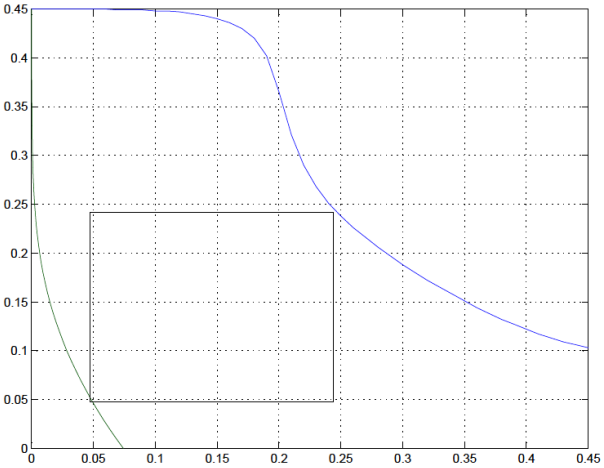

FIGURE 9 Butterfly curve for write operation at 45nm technology

V. CONCLUSION

Simulation and analyzation of performance of 6T SRAM cells at 180nm and 45nm technology for parameters like power consumption, delay and SNM is as desired. Simulation results shows clearly how read, write operation is performed.

VI. ACKNOWLEDGEMENTS

For power constrained projects like space exploration and satellites the SRAM cell which consumes minimum power should be used while for very fast processing devices the SRAM cell which has minimum time delay should be used. The SRAM cell which has maximum SNM can be used in the device which works in noisy environment. The design of SRAM cell can be optimized by tradeoff between various performance parameters. New design is not introduced within the project. In future we will propose new SRAM cell design or schematic, which decreases read/write delay, consumes less power.

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